Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A method for fabricating shallow trench isolation (STI) between deep trench capacitors, comprising the steps of:

providing a semiconductor substrate having thereon a pad layer, wherein the semiconductor substrate has a logic area and a memory array area and a plurality of deep trench capacitors are formed within the memory array area, and wherein each of the deep trench capacitors comprises a buried plate in the semiconductor substrate serving as one electrode of the deep trench capacitor, a storage node serving as the other electrode of the deep trench capacitor, a node dielectric layer between the buried plate and the storage node, and a collar oxide disposed at an upper portion of the deep trench capacitor;

studding a dielectric layer into a capacitor top recess on each of the deep trench capacitors, and the studded dielectric layer having a top surface that is coplanar with the pad layer;

depositing a buffer layer over the semiconductor substrate;

depositing a bottom anti-reflection coating (BARC) over

the buffer layer;

forming a photo mask defining memory array trench openings and logic area trench openings over the BARC;

through the memory array trench openings and logic area trench openings, dry etching the BARC, the buffer layer, the pad layer, and then etching into the semiconductor substrate selective to the dielectric layer and the collar oxide that both keep the deep trench capacitors intact, thereby forming isolation trenches between the deep trench capacitors within the memory array area and isolation trenches within the logic area;

stripping the photo mask and the BARC; and

filling the isolation trenches within the memory array area and the logic area with gap filling material.

[c2] 2.The method of claim 1 wherein the method of studding a dielectric layer into a capacitor top recess on each of the deep trench capacitors comprises depositing an HDPCVD oxide over the semiconductor substrate, and then chemical mechanical polishing the HDPCVD oxide stopping on the pad layer.

[c3] 3.The method of claim 1 wherein the pad layer is composed of silicon nitride.

[c4] 4.The method of claim 1 wherein the buffer layer is composed of silicon nitride.

[c5] 5.The method of claim 1 wherein the buffer layer has a thickness of about 500 angstroms.

[c6] 6.A method for fabricating shallow trench isolation (STI) between deep trench capacitors, comprising the steps of:
providing a semiconductor substrate having thereon a pad layer, wherein the semiconductor substrate has a plurality of deep trench capacitors formed therein, each of which comprising a buried plate in the semiconductor substrate serving as one electrode of the deep trench capacitor, a storage node serving as the other electrode of the deep trench capacitor, a node dielectric layer between the buried plate and the storage node, and a collar oxide disposed at an upper portion of the deep trench capacitor;
studding a dielectric layer into a capacitor top recess on each of the deep trench capacitors, and the studded dielectric layer having a top surface that is coplanar with the pad layer;
depositing a buffer layer over the semiconductor substrate;
forming a photo mask defining trench openings over the buffer layer;
through the trench openings, dry etching the buffer layer, the pad layer, and then etching into the semiconductor substrate selective to the dielectric layer and the

collar oxide that both keep the deep trench capacitors intact, thereby forming isolation trenches between the deep trench capacitors;
stripping the photo mask; and
filling the isolation trenches with gap filling material.

[c7] 7.The method of claim 6 wherein a bottom anti-reflection coating (BARC) is formed on the buffer layer.

[c8] 8.The method of claim 6 wherein the method of studding a dielectric layer into a capacitor top recess on each of the deep trench capacitors comprises depositing an HDPCVD oxide over the semiconductor substrate, and then chemical mechanical polishing the HDPCVD oxide stopping on the pad layer.

[c9] 9.The method of claim 6 wherein the pad layer is composed of silicon nitride.

[c10] 10.The method of claim 6 wherein the buffer layer is composed of silicon nitride.

[c11] 11.The method of claim 10 wherein the buffer layer has a thickness of about 500 angstroms.